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(54) Setting of decision thresholds and sampling phase based on previous bit values

(57) A decision feedback structure for recovering a bit stream out of received signals is contemplated, wherein the sampling instant may be tuned in dependence of the sequence or pattern of the preceding bits so as to follow the bit sequence dependent instant of the maximum eye opening. The decision-feedback equalizer structure comprises a signal input, decision means for making a bit value decision at a sampling instant, a feedback path to feed back bit values to said decision means and means for adapting the sampling instant for a bit value decision made by said decision means with respect to the sampling phase depending on the bit values of preceding bits, in particular depending on the bit value of the previous bit.

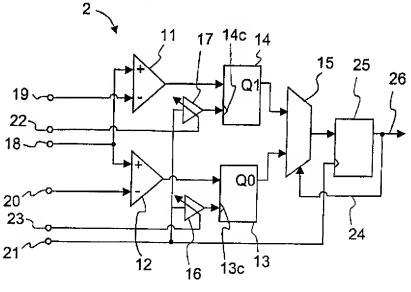

Fig. 3

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Description

[0001] The invention relates to a device and a method for signal equalization in a signal receiving unit comprising a Decision Feedback Equalizer, in particular to the adjustment of equalization parameters used to equalize the received signals and to a feed forward equalizer adapted to carrying out the adjusting method.

[0002] Modern high capacity, long distance communication systems are usually based on fiber-optical data transmission. However, the signals will become more or less distorted due to various linear and nonlinear phenomene upon transmission over the optical transmission fines. In particular, chromatic dispersion (CD), polarization mode dispersion, chirp, extinction ratio, four wave mixing, self phase modulation and cross phase modulation are relevant for the distortions end thereby introduce intersymbol interference (ISI). Additional distortions mey be introduced by various parasitic elements of the conversion circuitry.

[0003] Generally, these effects reduce the eye opening at the receiver and thereby lead to a reduced tolerable optical signal to noise ratio (OSNR).

[0004] In the optical receiver, the optical pulses are converted back into electrical signels. The digital data and sampling clock has to be derived from the analog signal by means of a clock end data recovery circuitry (CDR).

[0005] In order to improve the signal quality at the CDR circuit, it is known to apply adaptive equalization. The eye opening penalty caused by ISI may be reduced or removed by employing adaptive equelization, whereby the signal equalization is usually performed in the electrical domain of the optical receiver.

[0006] Additionelly, forward error correction is frequently applied in order to increase the transmission performance for e given signal to noise ratio. In encoding for forward error correction, redundant bits ere added to an incoming bit stream so that errors in transmission may be detected and corrected at the far end.

[0007] Different FEC-Coding-Schemes are used, such as so called in band or out band, BCH (Bose-Chaudhury-Hoequenghesn) or RS (Reed-Solomon) codes which fit for Sonet/SDH digital wrapper formats. If the input error rate of the data stream is below the error correction capability of the respective error correction code, the bit errors can be corrected and estimates of a bit error ratio (BER) mey be meesured by using tha additional information from the respective FEC-decoding scheme. Specifically, the number of errors that can be corrected emount to (d-1)/2, where d denotes the minimum number of bit positions by which code words for a particular code are different ("Hamming distance"). Thus, using FEC, the BER of the decoded output signels can be greatly reduced in comparison to the incoming signals received and converted by the optical receiver.

[0008] In order to increase the eye-opening before digitizing the received end converted signals, linear and non-linear equelizers are employed. Well known filters are feed forward equelizars (FFE) and decision feedback equalizers (DFE).

[0009] Particularly, decision-feedback equalization (DFE) is a widely-used technique for removing intersymbol interference whera noise enhencement caused by a linear fead-forward equalizer (FFE) may introduce performance problems.

[0010] In order to digitize the received signals, currently implemented DFE structures utilize a regular sampling phase derived from the recovered clock by means of a nerrowband clock recovery. Consequently, the derived sampling phase is slowly adepted and used for digitization of a large number of bits.

[0011] Howaver, the optimum sampling instant or phase may vary depending on the signal history. Particulerly, non-linear distortions may cause the position of the maximum eye opening to shift in time so that a CDR using a regular slowly varying sampling phase will miss the optimum instant for signal sampling.

[0012] Thus, it is an object of the invention to provide e decision feedback structure and e method for decision feedback equalization, wherein the sampling instant mey be tuned in dependence of the sequance or pattern of the preceding bits so as to follow the instant of the maximum eye opening.

[0013] Accordingly, the invention teaches a decision-feedback equeiizer structure to recover a bit stream out of received analog signals, which comprisss a signal input, bit value decision means for making a bit value decision at a sempling instant and a feedback path to feed back bit values to the decision means, whereby the structure further comprises means for adapting the sampling instant for a bit value decision made by the decision means with respect to the sampling phase depending on the bit values of preceding bits, in particular depending on the bit value of the previous bit.

[0014] Owing to the fact that esymmetrical distortions as introduced by nonlinear transmission effects require bit pattern dependent sampling phases to match the optimum eye opening, a gain of margin for OSNR penalty end receiver power penalty can be achieved by adapting the sampling instant accordingly. Thus, in contrast to prior art devices, the inventive decision-feedback equalizer structure provides for bit pattern controlled adjustment of the actual sampling phase. The instant to sample the received signal is selected end/or adjusted on the basis of a sampling phase derived from a clock recovery circle and a delay which is edepted in dependence of preceding bit velues. In order to select end/or edjust the actuel sampling instant for the present bit to be recovered, previous bit values are fed back by means of a feedback loop. By choosing appropriate adapting or adjusting parameters, the sampling instant or sampling phase for a present decision can be shifted to hit the instant of the maximum eye opening.

[0015] According to a preferred embodiment, the

means for adapting the sampling instant for bit value decisions comprise at least two tunable delay buffers for tuning a first sampling instant for bit patterns including a preceding zero bit and a second sampling instant including a preceding one bit.

[0016] By providing tunable delay buffers for different bit patterns, each buffer can be tuned independently to gain versatile adaptation of the delay parameters to the characteristics of the transmission line.

[0017] The data stream may include a forward error correction code (FEC) which allows to improve the bit error rate (BER) for a given signal-to-noise ratio (SNR) by reducing stochastic distortions from optical or electrical noise and cross talk. For high bit rate transmission, FEC becomes more and more mature to increase the tolerable SNR on long haul transmissions. In encoding for forward error correction, redundant bits are added to a bit stream so that errors may be detected and corrected at the far end. The number of added bits may be up to the number of signal bits, resulting in a doubling of the data transmission rate for in given channel. However, in many cases redundant transmission by using FEC is beneficial due to a guaranteed low error rate. During forward error correction, conditional bit error rates may be estimated. by counting faulty transmitted bits in dependence of preceding and succeeding bits. The ratios of conditional bit error rates provide information on deviations of decision thresholds and/or sampling phases from their optimum values. Likewise, these error rates may be used to shift the sampling instance. Ideally, if the values of decision thresholds and sampling phases are optimized, the conditional errors should be balanced. It is therefore advantageous to control the tunable delay buffers by conditional bit error rates estimated by forward error correction means.

[0018] The bit pattern dependent shift of the sampling instant may be transferred to the output signal which results in jitters of the clock of the output bit stream. In order to compensate this effect, the decision-feedback equalizer structure may advantageously comprise means for retiming the bit stream by using a clock signal recovered from the input signal.

[0019] Due to nonlinear distortions upon signal transmission, a bit pattern dependent shift of the level of the optimum decision threshold occurs in addition to the bit pattern dependent shift of the instant of the maximum eye opening. Therefore, it is advantageous to provide means for adaptively tuning the decision threshold for bit value decisions in dependence of the bit value of the preceding bit in order to gain optimum decision conditions.

[0020] Within the scope of the present invention, it is also contemplated to provide a method of recovering a bit stream from a received analog signal in a decision feedback structure. According to the method, a clock signal is recovered from the received analog signals, a sampling phase is generated from the clock signal, the input analog signal is compared with a decision threshold to come to a bit value decision at a time instant and a bit stream is generated on the basis of the bit value decisions, whereby the instant is adapted with respect to the sampling phase depending on previous bit value decisions, in particular depending on the preceding bit value decision.

[0021] Consequently, the method is appropriate to provide optimum performance for accurate recognition of transmitted bit sequences which have been subjected to nonlinear effects since the optimum sampling instant is strongly influenced by ISI.

[0022] Advantageously, the instance may be tuned by means of conditional bit error rates which have been estimated by forward error correction.

[0023] According to a preferred embodiment, two sampling instants are tuned independently. More specifically, a first sampling instant is tuned which is utilized for the bit value decision if the preceding bit value is zero and a second sampling instant is tuned which is utilized for the bit value decision if the preceding bit value is one. For example, the tuning parameters may be controlled by the conditional bit error rates as estimated by forward error correction.

[0024] Owing to bit pattern or bit history dependant sampling phases, the bit period of the digitized output data may oscillate. Thus, In order to avoid this undesirable affect, it is advantageous to synchronize the output data. The synchronization may be advantageously accomplished by a retiming procedure using the clock recovered from the input data.

[0025] In order to improve the performance of the method, it is further advantageous to adaptively tune the decision threshold for a bit value decision in dependence of the bit value of the preceding bit.

[0026] The invention is described in more datail below in view of preferred and most preferred embodiments and reference is made to the accompanying drawings, in which

Fig. 1 is a schema of an optical transmission channel,

Fig. 2 shows eye diagrams of distorted signals, and

Fig. 3 depicts a schematic circuit diagram of a preferred embodiment of the invention.

[0027] Rafarence is now made to Fig. 1 showing components of an optical transmission channal 1, wherein the inventive feedback equalizer structure may be employed. Before transmission, data are processed in an FEC encoder 3 to provide a redundantly coded bit stream. The Bit stream is converted into optical signals by means of a electrical to optical converter 4 and transmitted via a fiber 5 to tha receiver at the far end. The receiver comprises an optical to electrical converter 6 and clock and data recovery circuitry 7 including a signal equalizer. The FEC-coded bit stream is than decoded

by means of decoder 8. The decoder 8 may additionelly monitor the transmission performence. The monitoring paramaters, such as integral or conditional BER's mey be used to adept or tune the settings of other components of the transmission line. In particular, the signal equalizar et the receiver's side has to be adapted to variations in the transmission characteristics of the line.

[0028] However, due to nonlinear optical effects in the fiber, the optical signals errlving at the far end are more or less distorted end subjected to ISI, es discussed above.

[0029] Fig. 2 shows eye diegrams of distorted signals corresponding to verious bit sequances. The arrows 9 end 10 indicate the maximum eya openings for signals having different signel histories. More detailed, arrows 9 end 10 denote the maximum eya opening for signel sequances heving a preceding zero bit and one bit, respectively. Dashed lines 91 and 92 merk optimum decision thresholds for signals corresponding to bit sequences having a preceding zero bit (a010, e001) and a preceding one bit (a101, a110), respectively. Currently implemented DFE structures edept the decision threshold level in dependence of the bit sequence to compensate this effect introduced by ISI.

[0030] However, es it is evidant from the position of the arrows 91 end 92, the time instant of the maximum eya opening shifts depending on the signel history, too. In the case of e leading zero bit, the optimum instant lies at time t0, whereas a leading one bit shifts the instant to time t1. The DFE structure according to the present invention is capable to adapt the sampling instant depending on the signal history, resulting in an improved perfomance.

[0031] Reference is now made to Fig. 3, showing a schematic circuit diagram of an exemplary one-tap embodiment of the inventive DFE structure 2. Data transmitted via an optical fiber ara received as analog signals at input 18 efter optical to electrical conversion. A clock signel ganarated by e clock recovery circuit is supplied via clock input 21. Input analog signals received at input 18 are converted into binary signels by means of comparators 11 and 12. Each of the comparators 11 and 12 is supplied with independent decision threshold signels vie threshold inputs 19 and 20, respectively. In datail, comparator 12 is supplied with a decision threshold signal appropriete for bit sequences with a preceding zero bit and comparator 11 is supplied with e decision threshold signal appropriate for bit sequences with e preceding one bit. The threshold levels may be tuned in dependence of conditional bit error rates estimated by forward error correction means.

[0032] The binary output signals of comparators 11 and 12 are supplied to flip-flops 13 and 14. Preferably, flip-flops 13 and 14 are D-flip-flops. Signal sampling of the flip-flops is triggered by means of clock signals provided vie clock inputs 13c end 14c, respectively. The clock signels are tapped from the clock signal recovered from the input data and supplied vie clock input 21. The tapped clock signal is delayed by means of tuneble deley buffers 16 and 17. In this way, input signals tapped via branch 18e are sampled using a sampling instant generated from the sampling clock by tunable delay buffer 17. The sampling clock is delayed appropriately to match the best sampling instant corresponding to bit sequences with e leading one bit (instant t0 in fig. 2). Similerly, input signels tapped via brench 18b are sampled by flip-flop 13 using a sampling phese generated from the sampling clock by tuneble deley buffer 16.

[0033] The deley generated by buffers 16, 17 is controlled by tuning parameters such as tuning volteges supplied via inputs 22 and 23, respectively. Tha tuning parameters ere adepted to the characteristics of the transmission line. In example, the deley buffers 16 and 17 mey be tuned in dependence of conditional bit error rates which heve been estimated by forward error correction so es to meintain optimum sampling conditions. Alternetively, the parameters mey be tuned using look up table values. The table velues may be calculated by means of an eya monitor or an analog-to-digital converter (ADC) and a least mean square elgorithm.

[0034] At the output of flip-flops 13 end 14, digitized signals Q0, Q1 are provided, which ere fed into multiplexer 15. In the multiplexer 15, output signels ere generated by releying one of the digitized signels Q0 and Q1. By means of a feedback path 24, the preceding bit signal is fed back into the multiplexer 15. A relaying decision is made on the basis of the preceding bit value, i. e., in the case of a preceding zero bit, signal Q0 is releyed, whereas signal Q1 is releyed in the case of a preceding one bit.

[0035] Due to the releying operation of multiplexer 15, the output signals comprise a clock signal which is a superposition of the delayed clock signels generated by tuneble deley buffers 16 and 17. Consequently, the clock of the output bit stream includes a jitter which may cause interference with consecutive data processing devices such as forward error correction circuitry. In order to avoid undesirable effects due to clock jitter, the DFE structure2 further provides for data retiming or synchronization. Retiming is accomplished by e further flip-flop 25 connected to the output of the multiplexer 15. Flip-flop 25 is triggered by the clock signel as recovered by the clock recovery circuitry of the receivar and supplied vie clock input 21. In this way, a reguler bit period in the output bit stream is obtained.

[0036] The embodiment described above is a one-tap DFE-structure. However, the concept of the DFE structure according to the present invention can be eesily extended to multi-tap DFE-structures, whereby each tap corresponds to e specific sequence of preceding bits or a group of sequences of preceding bits.

Claims

1. A decision-feedback equalizar structure for recov-

ering a bit stream out of received signals, comprising:

- a signal input,
- decision means for making a bit value decision at a sampling instant,
- a feedback path to feed back bit values to said decision means,

characterized by

- means for adapting the sampling instant for a bit value decision made by said decision means with respect to the sampling phase depending on the bit values of preceding bits, in particular depending on the bit value of the previous bit.

2. A decision-feedback equalizer structure according to claim 1, whereby the means for adapting the sampling instant for bit value decisions comprises at least two tunable delay buffers for tuning a first sampling instant for bit patterns including a preceding zero bit and a second sampling instant including a preceding one bit.

3. A decision-feedback equalizer structure according to claim 2, whereby the at least two tunable delay buffers are controlled depending on conditional bit error rates estimated by forward error correction means.

4. A decision-feedback equalizer structure according to one of claims 1 to 3, **characterized by** means for retiming said bit stream using a clock signal recovered from the input signal.

5. A decision-feedback equalizer structure according to one of claims 1 to 4, further comprising means for adaptively tuning the decision threshold for bit value decisions in dependence of the bit value of the preceding bit.

6. A method of recovering a bit stream from a received analog signal in a decision feedback structure, comprising the steps of:

- recovering a clock signal from the received analog signals,
- generating a sampling phase from the clock signal,
- at an instance comparing the analog signal with a decision threshold to come to a bit value decision,
- generating a bit stream based on said bit value decisions,

characterized by the step of

- adapting said instance with respect to the sampling phase depending on previous bit value decisions, in particular depending on the preceding bit value decision.

7. A method according to claim 6, whereby the step of adapting said instance with respect to the sampling phase comprises the step of tuning said instance in dependence of conditional bit error rates estimated by means of forward error correction.

8. A method according to claim 6 or claim 7, whereby the step of adapting said instance with respect to the sampling phase comprises the steps of

- tuning a first sampling instant which is utilized for the bit value decision if the preceding bit value is zero and
- tuning a second sampling instant which is utilized for the bit value decision if the preceding bit value is one.

9. A method according to one of claims 6 to 8, further comprising the step of retiming said bit stream using a clock signal recovered from the input signal.

10. A method according to one of claims 6 to 9, further comprising, the step of adaptively tuning a decision threshold for a bit value decision in dependence of the bit value of the preceding bit.

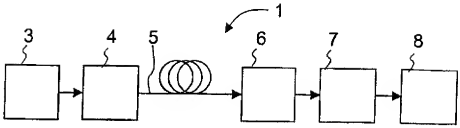
1
3
4
5
6
7
8

Fig. 1

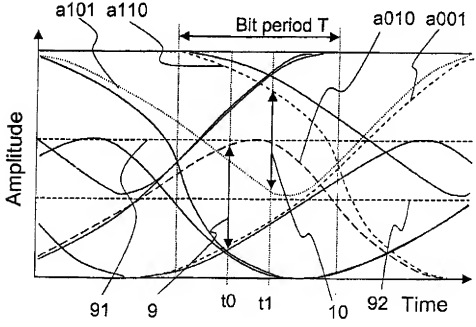
a101 a110
Bit period T
a010 a001
Amplitude
91
9
t0
t1
10
92
Time

Fig. 2

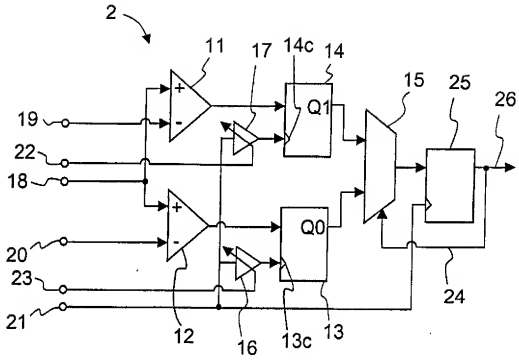

Fig. 3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 25 0544

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	5 July 2002	Moreno, M

CATEGORY OF CITED DOCUMENTS

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EUROPEAN SEARCH REPORT

Application Number
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